REMARKS/ARGUMENTS

The foregoing amendment makes this application a continuation-in-part of applicants' copending application Serial No. 10/067,372 (Publication No. 202/0120896).

In addition, applicants respectfully traverse the Examiner's denial of domestic priority on the ground that the provisional application Serial No. 10/067,372 does not have a reference to "global scan enable and global set/reset enable signals." In this regard, the Examiner's reference is made to applicants' provisional specification, page 3, first full paragraph reading:

> The present invention uses a scan enable (SE) and and/or gate to disable the asynchronous set/reset signals of all scan cells. A new set/reset enable (SR_EN) signal is introduced to propagate the faults of asynchronous set/reset signals in a dedicated capture cycle. In this dedicated capture cycle, the test clocks are disabled so that the race conditions that exist on prior-art #3 are eliminated. The present invention repairs the asynchronous set/reset violations either at the register transfer level (RTL) or the gate-level circuit.

Also, applicants' SUMMARY of the invention at page 4 reads as follows:

Three additional input signals, a scan enable signal SE a test enable signal TE and a set/reset enable (SR_EN) signal can be added to the RTL codes for this purpose. The three enable signals, SE, TE, and SR_EN will be used to control the operation of added scan logic so that the circuit can function correctly during scan and normal operations. The following table summarizes the circuit operation mode under different SE, TE, and SR_EN values. The test clocks are disabled during the capture set/reset mode.

TE	SE	SR_EN	Mode
0	0	1	normal
1	1	x	shift
1	0	0	capture data
1	0	1	capture set/reset

These all imply that the scan-enable SE signals and the set/reset enable SR_EN signals are global in nature.

Furthermore, the second full paragraph on page 7 of applicants' provisional specification clearly implies that the scan-enable signal SE and the set/reset enable signals (SR_EN) are global in nature.

Furthermore, the second full paragraph on page 9 of applicants' provisional application clearly implies that the scan-enable signal SE and the set/reset SR_EN signal are global in nature.

Furthermore, the first full paragraph on page 12 of applicant's provisional application clearly implies that the scan-

enable signal SE and the set/reset signals, in the first stage of capture operation SR_EN, is global in nature.

Finally, claim 6 of applicants' provisional application contains language clearly implying that the scan-enable signals and the set/reset enable (SR_EN) signals are global in nature.

In view of the above and the amendment making this application, insofar as the global nature of the scan enable and set/reset enable SR-EN signals are concerned, entitled to the filing date of the provisional application and Wang et al Pub. No. 2002/0120896, applicants have mooted the rejection based on Wang et al Pub. No. 2002/0120896 and have antedated the ORCA® Series 4 FPGAs by Lattice Semiconductor reference.

In view of the above, further and favorable reconsideration is respectfully requested.

Respectfully submitted,

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Date: December 12, 2005